AD-A222 630

VLSI Technol Symp '90

ROLE OF SURFACE PASSIVATION IN THE INTEGRATED PROCESSING OF MOS STRUCTURES

M. Offenberg, M. Lichr, S.R. Kasi, and G.W. Rubloff
IBM Research, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598, USA

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Introduction

In order to achieve low defect densities and process simplification, future ULSI manufacturing is expected to incorporate multichamber integrated vacuum processing equipment. This raises opportunities for new levels of contamination control, including microscopic reactive impurities as well as particles, but also introduces new questions about how to successfully integrate process steps such as preoxidation cleaning with thermal oxidation.

In this paper we describe electrical properties of simple MOS capacitors prepared in a multichamber integrated ultrahigh vacuum (UHV) processing system with in-situ analysis capabilities [1]. This system has allowed us to integrate the surface preclean steps with the thermal oxidation process *without* air exposure between the two. In-situ surface analysis has permitted characterization of the precleaned surface, particularly the concentration of oxide and carbon present after different precleaning treatments.

The results demonstrate that *integration of preclean and oxidation* can yield MOS structures with device quality dielectric breakdown characteristics. Furthermore, they indicate that the role of low level reactive impurities becomes crucial when using integrated vacuum processing systems. Intentional introduction of a thin passivating oxide layer is essential prior/during wafer heating to oxidation temperature; this prevents degradation of electrical quality which appears associated with etching and roughening of the Si surface by trace O_2 impurities.

Experimental

RCA-cleaned p-Si(100) wafers (1 Ω-cm) were introduced into a N_2-purged glove box, where final cleaning processes were performed, including:

- HF dip (10″ in 1:10 HF solution)
- vapor HF exposure (5′ over HF solution)
- uv/ozone treatment (10′ in O_2 with Hg radiation)
- H_2O_2 immersion (10′ in 1:5 H_2O_2:H_2O solution at 60°C)

Control wafers were those with none of these final steps.

Following preclean in the glove box, wafers were transferred through UHV to a UHV-based (10^{-8} torr base pressure) oxidation reactor, so that *no air exposure* was incurred between the final preclean and the thermal oxidation steps. The reactor was then vented to atmospheric pressure using ultrapure Ar or O_2, and the wafers were pushed slowly into the hot zone of the furnace. In some cases a 10′ preanneal in Ar was carried out at various temperatures before the oxidation (2h at 830°C, yielding ~12nm SiO_2) and post-oxidation anneal (20′ in Ar, then 1′ in O_2). Al contacts (16 mil dia) for MOS structures were deposited after wafer removal from the integrated system. Auxiliary measurements were made on wafers oxidized in a standard clean room oxidation furnace. Surface concentrations of oxide, carbon, and fluorine resulting from the final preclean treatments were measured using integrated surface analytical tools.

Results and Discussion

Fig. 1 displays breakdown statistics for three cases when warm-up to oxidation temperature was carried out in Ar. The control shows good breakdown statistics (mean breakdown field ~12MV/cm) and some low field events.

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The HF-dipped wafer (which showed no oxide after preclean) yielded poor breakdown behavior (~3 MV/cm), while sequential HF dip followed by uv/ozone treatment (leaving a thin ~1nm oxide after preclean) gave good breakdown characteristics (~ 13 MV/cm).

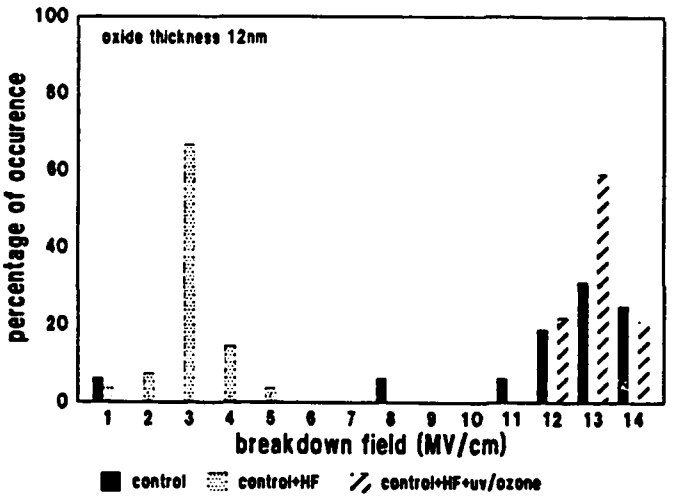

Fig. 1. Breakdown histogram for integrated preclean and oxidation treatments, cf. control.

These results suggest that the presence of oxide before carrying out oxidation *in an integrated process* is critical for oxide electrical quality. We verified this systematics with other pretreatments:

- Poor breakdown behavior was obtained when the final pretreatment left *no* oxide (vapor HF, in-situ epitaxial Si growth, as well as HF dip).
- Good breakdown behavior was found when oxide *was* present (uv/ozone, H_2O_2 immersion, as well as control/RCA clean).

We believe that the oxide produced by pretreatment is effective because it prevents a deleterious etching and roughening of the Si surface by trace oxygen impurities. Smith and Ghidini [2] showed that sufficiently low concentrations of O_2 cause *etching* of the Si surface, as opposed to oxidation at higher concentration. The critical O_2 pressure separating etching from oxidation increases with increasing temperature. Since etching is a statistical event, one must expect consequent roughening of the Si surface. For thin oxides this roughness will be translated to the Si/SiO_2 interface, where degradation of breakdown characteristics would be expected [3].

This suggestion is supported by the following observations for HF-dipped precleans. For warm-up in 1 atm. O_2, where oxidation rather than etching will occur, good breakdown behavior is obtained, in contrast to warm-up in Ar. If an anneal in Ar (with trace oxygen present) is carried out before this oxidation, we expect etching and roughening of the clean surface to influence subsequent oxide quality and to be more severe for higher Ar anneal temperature [2]. Fig. 2 demonstrates precisely this behavior.

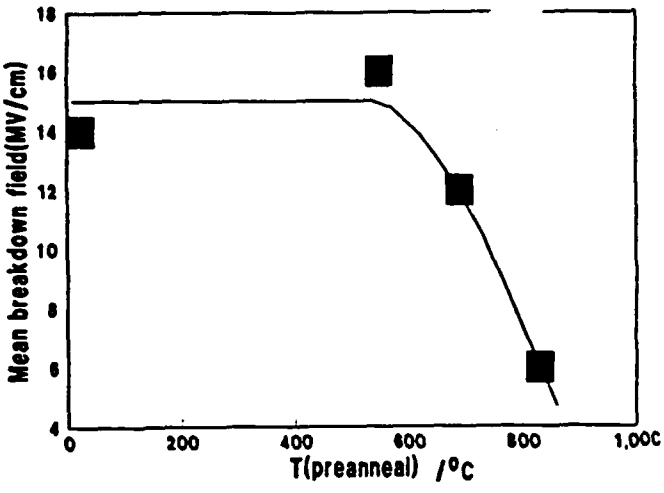

Fig. 2. Dependence of mean breakdown field on Ar preanneal temperature for HF-dip final preclean, Ar preanneal (10'), cooling, and warm-up in O_2 .

Further evidence for roughening by the etching reaction during nominally inert ambient annealing has been found by low energy electron diffraction (LEED) studies. The Ar preanneal produced more diffuse diffraction spots in the Si surface LEED pattern on HF-dipped wafers than on control wafers, indicative of larger roughness in the former case.

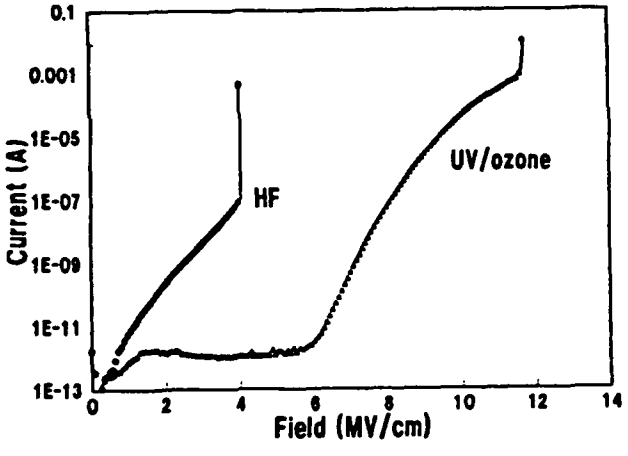

Fig. 3. Current-voltage characteristics of HF-dipped and control wafers, showing an increase in low-field leakage for Ar preanneal.

Current-voltage characteristics of HF-dip pretreated MOS capacitors are given in Fig. 3. For Ar preanneal of oxide-free wafers (HF-dip preclean), the onset of the tunneling current is displaced to lower fields, whereas this behavior is not observed for the oxide-covered (control) wafers. This can be interpreted as field-enhancement due to roughness [3] at the Si/SiO_2 interface, consistent with the proposed etching mechanism. Moreover, electron injection from the Si substrate results in even lower fields for onset of tunneling than does injection from the metal.

We also investigated other conceivable sources for the poor breakdown behavior on an HF etched sample. Particle densities, their compositions (measured by energy-dispersive x-ray analysis), and overall surface impurity levels (C, F, measured by x-ray photoemission) were very similar for HF-dip and uv/ozone preclean treatments. This indicates that neither particles nor low level reactive impurities are responsible for the systematics observed here between breakdown and preclean treatment.

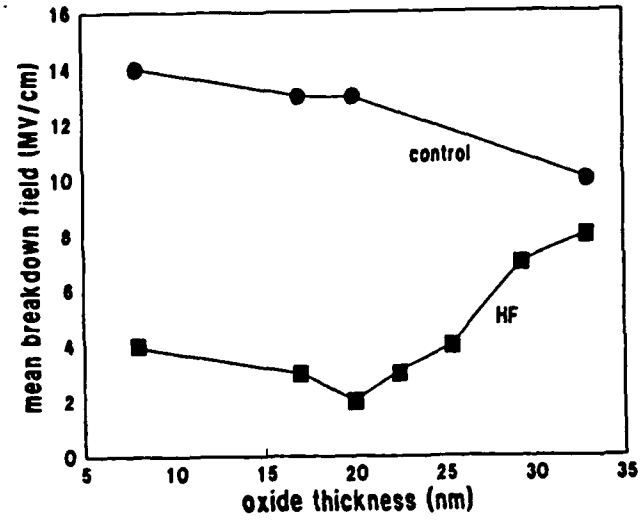

Fig. 4. Mean breakdown field as a function of oxide thickness for HF-dip precleaned wafers compared to controls.

As shown in Fig. 4, the breakdown degradation is more severe for thinner oxides, which are crucial for ULSI. Even in the case of ~30 nm oxide, low field breakdown events are significantly more frequent for the HF-dip preclean than for the control. Finally, there seems to be some improvement with oxide thickness, presumably due to increasing ratio of oxide thickness to average roughness.

Conclusions

We have shown that integration of final preclean with thermal oxidation can lead to operative MOS structures with good breakdown behavior. The use of vacuum transfer for this integration prevents air exposure between steps, but also requires specific recipes. In particular, the presence of trace amounts of oxygen, even in ultraclean systems, requires intentional passivation of the surface in order to prevent etching and roughening. This passivation can be accomplished either by warm-up in oxygen for the oxidation process or by fabrication of a thin oxide layer as part of the integrated cleaning step.

We appreciate the assistance of S. Cohen and A. Parsons in these studies. This work was supported in part by the Office of Naval Research.

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